International Journal of Computer Architecture and Mobility
(ISSN 2319-9229) Volume 3 -Issue 1, January 2015

New Design Approach of Flash ADC

R.B. Gaikwad[1], Navneet Nagar[2]

Department of Electronics and communication Ujjain Engineering Collage Ujjain India

rambhaugaikwad@gmail.com[1]navneetnagar09@gmail.com[2]

Abstract:- This paper describes the design and implementation of a Low Power 3-bit flash Analog to Digital converter (ADC). It includes 7 comparators and one thermometer to binary encoder. It is implemented in 0.18um CMOS Technology. A design method for flash ADC is presented. With an inverter as a comparator along with an NMOS and a PMOS as switches, we use bisection method to let only half of comparators in flash ADC working in every clock cycle. For example:-
A 3-bit flash ADC, with a maximum acquisition speed of 1 GHz, is implemented in a 1.2 V analog supply voltage. LTSPICE simulation results for the proposed flash ADC verifying the analytical results are also given. Flash ADC consumes about 30 mW in a commercial 180 nm CMOS process. The new design offers lower number of comparators and lower power consumption compared with the traditional flash ADC. The power consumption of proposed circuit is only 15 mW with LTSPICE simulation Compared with the traditional flash ADC, our bisection method can reduce up to 50% in power consumption.

Introduction:-

The A/D converters play an important role between analog and digital signals. The flash ADC is a frame of AD converters having very high data conversion speed , low-resolution and large chip area along with large power dissipation. The flash ADC architecture uses 2"-1comparators to convert an n-bit data without the requirement of sampling-and-hold circuits. Fig. 1 shows an example of a traditional flash ADC architecture.
In a flash ADC, comparators generate an output pattern called a thermometer code. According to the thermometer code, the bubble error corrector followed by the encoder can generate the digital binary outputs. When the comparators' outputs were unknown and passed through the encoder of ADC, the meta-stability errors [5] would occur. The 2"-1comparators in flash ADC also cost too large area and lead much power consumption.
To overcome the above problems, we got an idea from bisection method to let only half of comparators working in every clock cycle for reducing the power consumption.
Our proposed circuit and its operation are examined in Section 11. In Section 111**,** the simulation results with LTSPICE are demonstrated. Finally, the conclusion is provided in Section IV.

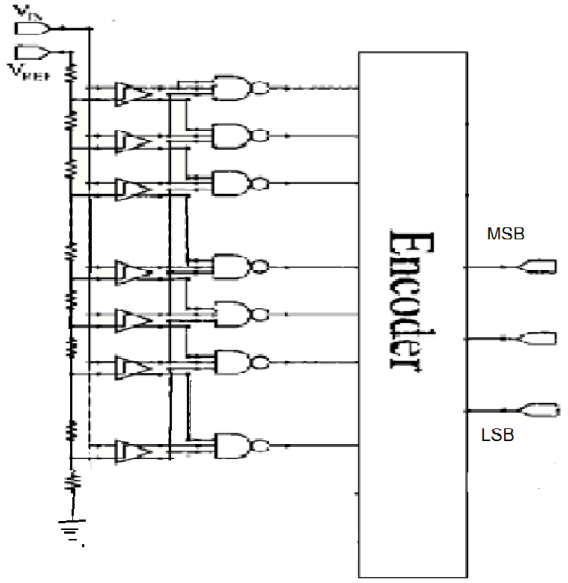

Fig:1 3 bit Traditional Flash ADCs

Proposed Method:-

In the design process of the ADC, there are many challenges, and the challenges look different depending on the ADC architecture that is implemented. As we know, the thermometer codes of flash ADC are composed of series 0 and 1 generated by comparators, as

shown in Fig. 2. The bubble error corrector is used to detect and correct possible bubble error codes. The final digital outputs are determined by the interface of 0 and 1 of thermometer codes after passed the encoder. As shown in Fig.3, if Vin<Vref, the upper half of thermometer codes will be set all 0. If Vin > Vref, the lower half of thermometer codes will be set all 1.

Based on the above induction, when Vin<Vref, we make the upper half of comparators' outputs to be all 0 and keep the lower half of comparators to still make comparison between input and reference voltages. Equivalently,

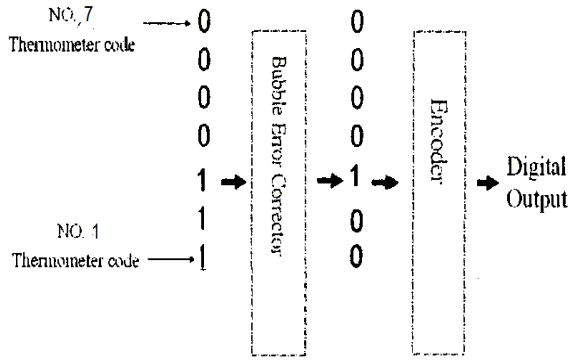

Fig 2 Thermometer Code

when Vin > Vref, we make the lower half of comparators' outputs to be all 0 and keep the upper half of comparators to still compare input and reference voltages. Because we have no idea to make the lower half of comparators' outputs to be all **1,** we can only make them to be all 0. Based on our figure out, when thermometer codes pass through the bubble error corrector, the outputs of bubble error corrector are correct, as shown in Fig. **2.** With using the bubble error corrector the outputs of lower half of comparators can be also corrected.

With the above figuration, we use a comparator-based inverter Inv. along with an NMOS and a PMOS as switches, referred in Fig. 4 for a 3-bit flash ADC, to control the clock entering to Comparators. To make well control to comparators, we size the inverter to determine whether the clock passed to the comparators or not.

An illustration shown in Fig. 5, when the flash **ADC** with Vin < Vref/2, we make the output thermometer codes of comparators No.6 - No.7 to be all 0 by stopping to inject the clock into the upper half of comparators to make them having no outputs, but the lower half of comparators still make comparison with input voltage and reference voltage.

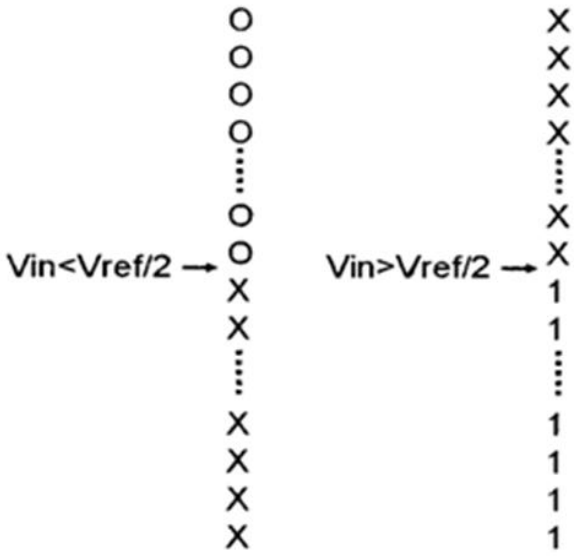

Fig3Thermometer code of Vin<Vref and Vin>Vref

By at current time, the output of the comparator-based inverter **Inv** will be logic high and the switches NMOS MI is on and PMOS M2 is off. Vref, as shown in Fig. 6, we make the output thermometer codes of comparators No.1- No.2 to be all 0 by stopping to inject the clock into the lower half of comparators to make them having no outputs, but the upper half of comparators still make their

normal comparisons. Meanwhile, the inverter's output will be logic low and the same time switches NMOS M1 is off and PMOS M2 is on.

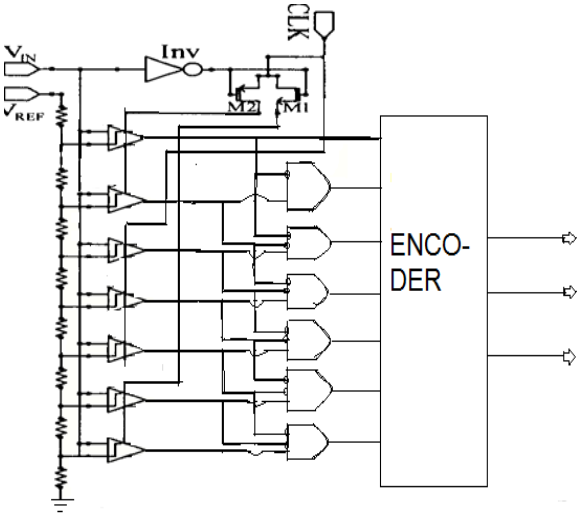

Fig:4 Proposed 3 bit Flash ADCs

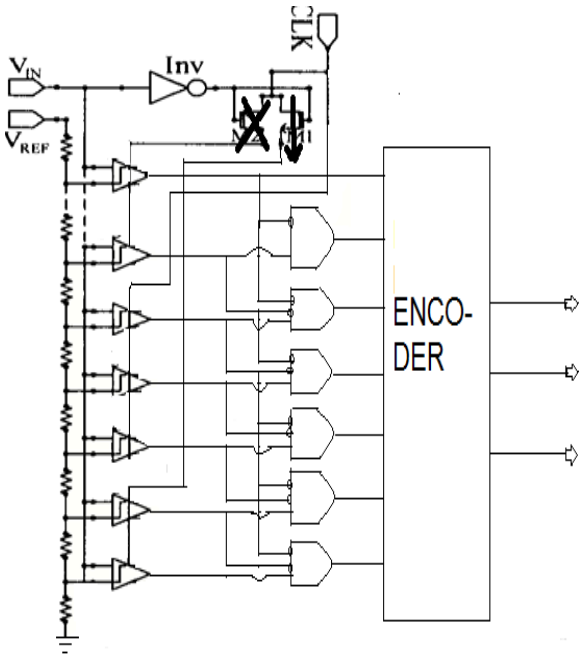

Fig 5 Operation Of 3 bit Flash ADCs at Vin<Vref

In order to make the outputs of bubble error correctors having applicable accuracy, we don't cut off the clock of comparators No.3 - No.5 that can get the correct digital outputs. To procure our above idea, we design a comparator- based inverter associated with two switches and then the bisection operation mode of controlling upper and lower comparators is formed. When Vin < Vref the input signal will be inverted and leads the **NMOS** M1 on. When Vin > Vref, the input signal will be inverted and leads the PMOS M2 on.

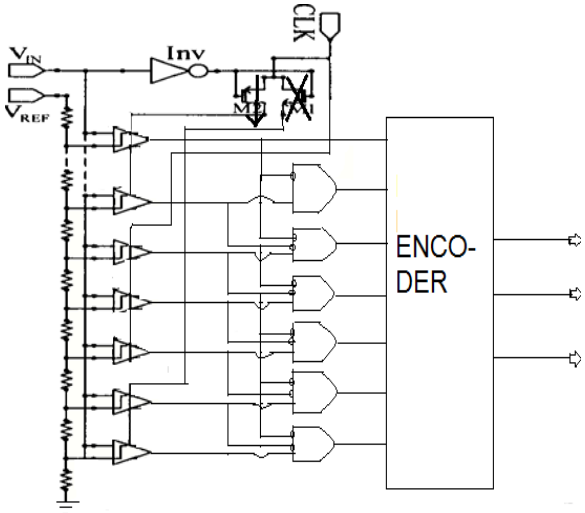

Fig:6 Operation of 3 bit Flash ADC at Vin>Vref

Comparator:-

Figure 7 shows comparator which is a predefined in LTSPICE simulator. It provides rail to rail output to the digital part of ADC.

A fast reset scheme is introduced by resetting the output through two parallel discharge paths. During the negative half cycle of the clock, the switching transistor M1 is turned on and the output discharged which forcus the output (vout+ - vout-) to be zero. While in the positive half cycle of the clock, the switch is turned off which allows the comparator to evaluate its differential input and generate the corresponding differential output which is either VDD or –VDD.

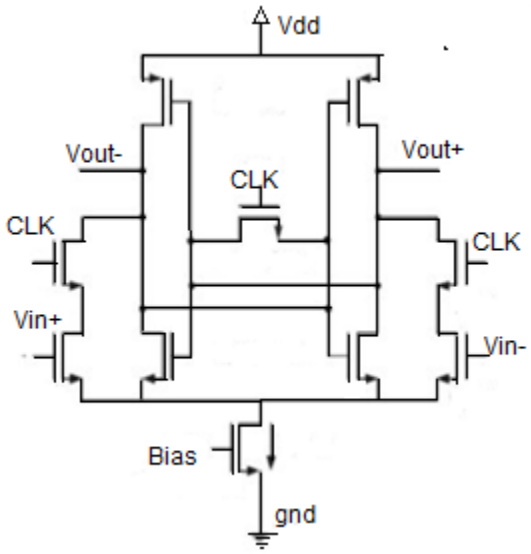

Fig:7 Comparator

Simulation Result:-

Simulation of our above idea and presents the input and output signals of the comparator-based inverter. Comparator is always negative during the positive half cycle. In the negative half cycle the differential output is discharged. The layout of the main modules comparator is shown in Fig 8 . The performance of the proposed architecture is characterized by computing its figure of merit.

$$\textbf{FOM} = \frac{2^{N\,bits} * Fsample}{Pdiss}$$

To make sure our proposed method to a flash **ADC** that can reduce power consumption. The power saving is up to 44%. The results is approved the effective of our bisection method. The DNL and INL of our proposed flash ADC are shown in Fig. 9 and Fig. 10, respectively. Their linearity is well controlled within ± LSB.

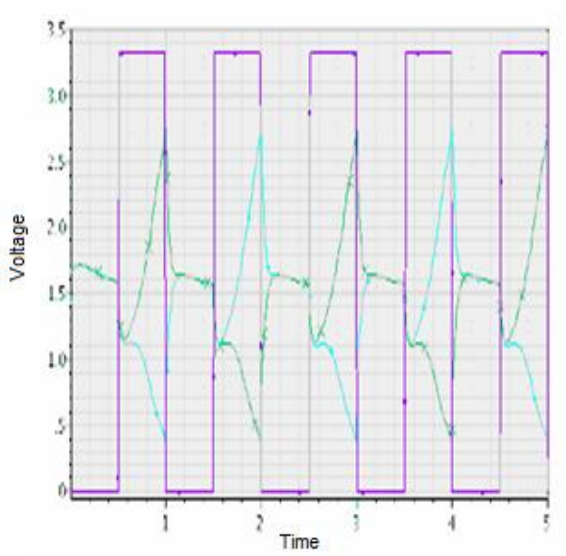

Fig: 8 comparator simulation results

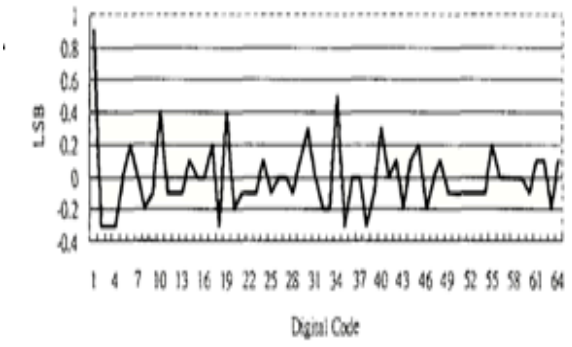

Fig. 9 *The DNL of our proposed flash ADC*

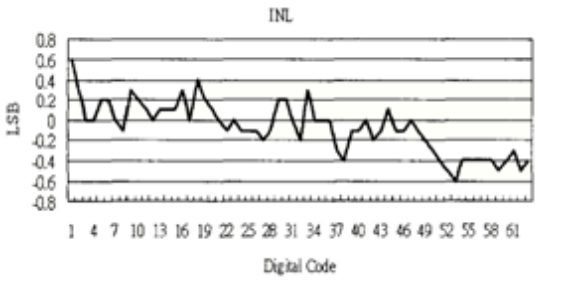

Fig. 10 The INL of our proposed flash ADC

Conclusion:-

A new power saving design method for a CMOS flash ADC is presented. Our proposed circuit needs only a comparator-based inverter along with an NMOS and a PMOS as switches for operating bisection modes to comparators. The power saving of near 85% matches our prediction that shows the encourage. Experimentally, the inverter size is dominated that is needed to size carefully for the digital output.

References:-

1. *Design Considerations for Interleaved ADCs Behzad Razavi, Fellow, IEEE2013*
2. *1-GS/s 6-bit flash ADC in 90 nm CMOS Shaker, M.O. Center for Adv. Comput. Studies, Univ. of Louisiana at Lafayette, Lafayette, LA, USA*
3. *Capacitive Interpolated Flash ADC Design Technique ieee2010*
4. *A 6-bit CMOS inverter based pseudo-flash ADC with low power consumptionHe Tang, Hui Zhao, Xin Wang, Lin Lin, Qiang Fang, Jian Liu and Albert Wang* Dept. of EE, University of California, Riverside, USA, ieee2013*
5. *H. Tang1, H. Zhao1, S. Fan2, X. Wang1, L. Lin1, Q. Fang1, J. Liu1, A. Wang1* and B. Zhao2 Dept. of Electrical Engineering, University of California, Riverside, CA, ieee2010*
6.