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WIRELESS VISION SENSOR NODE BASED on FPGA

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***ABSTRACT*------ The low-power consumption remote Industrial security alarm system developed by applying WSN, FPGA and GSM technology is presentedThe recent advances in the embedded system, semiconductor and sensor system have made it possible to develop a efficient, low power vision sensor. Security and surveillance are one of the most popular sectors that need better and effective products to be developed everyday. Wireless vision sensor node has many applications in these sectors and many future improvements can be made for applications in different fields . The wireless sensor makes resourceful use of FPGA, image acquisition block and transmission block. The system has the ability of collecting, wireless receiving and sending data and the output giving an image of area under surveillance for further action to the user's mobile phone when some dangerous condition has been detected. It is seen from the results that the system is feasible.**

Keywords **---- FPGA,GSM, wireless, security, mobile phone**

I. INTRODUCTION

Visual information is the most intuitive information perceived by human. Image sensors are able to provide the visual information for recognition, monitoring and surveillance. Networks of visual sensors are the solution of choice for a number of societal, research, and educational applications. Architectural challenges are posed for designers of image sensor nodes such as computational power, energy consumption, energy sources, communication channels, and sensing capabilities. We discuss the characteristics and requirements for an image sensor node. An image sensor node is designed and implemented for wireless sensor network. It includes anFPGA processor, memory image acquisition unit, GSM module and power unit etc. Thus this node has its application in various areas of interest such as health monitoring, security, scrutiny, record tracking, etc. And the design is such that can have many more addons to examine other factors to create complete surveillance system.

In today's world most sensing applications require some form of digital signal processing and these are implemented primarily on serial processors. While the required output is achievable, it can be beneficial to take advantage of the parallelism, low cost, and low power consumption offered by FPGAs (VIRTEX 5). The Field Programmable Gate Array (FPGA) contains logic components that can be programmed to perform complex mathematical functions making them highly suitable for the implementation of matrix algorithms. The use of FPGA makes it possible to develop most of the system in on block including the controller, memory, transmitter. FPGA has main advantage that it requires lesser power and the complete implementation will thus reduce total power required and a low power compact system can be developed.

In this paper, implementation of such a wireless vision sensor node is described that is efficient and effective in most aspects of recent requirement like less space, power and easy implementation. No external memory is used in the processing. The FPGA used has sufficient block RAM to store a image. This reduces the problem of interfacing external memory, matching its clock, lesser hardware and extra power. The remaining paper is structured as follows: In the section II has a literature survey. In section III, converses the architecture and design of the wireless vision node. Section IV has implementation of the node. In Section V, we show the simulation and real experimental results, section VI complications and future implementations and section VII concluding the paper.

II. LITERATURE SURVEY

The vision sensor have been developed earlier are connected to the controller and transmit data through wire.
Used external memory for storage. The continuous image transmission of the video requires continuous use of the channel and has large memory requirements. Different controllers were used for different parts of the node increasing the hardware and other difficulties.

Thus this wireless sensor would surely reduce the wiring and connection difficulties and make it easier to install the sensor at any remote place increasing the

convenience and worth of the sensor. The vision sensor developed here sends image after specified interval reducing the complexity of the project largely. And as the complete controller is implemented on the same FPGA unit creating a all in one controller though makes some complications in programming but finally gives a singly controlled system with all action taken by same controller making it easy to modify and further expansion.

III. ARCHITECHTURE AND DESIGN

To accomplish the target of easily configurable, low power and a compact vision sensor node we surely need the heart of the system to have various capabilities to fulfil most of the requirements. So the FPGA used here is VIRTEX5 on which a complete system is developed managing each aspect in well organised way. Here is the block diagram of the system showing main blocks of the system.

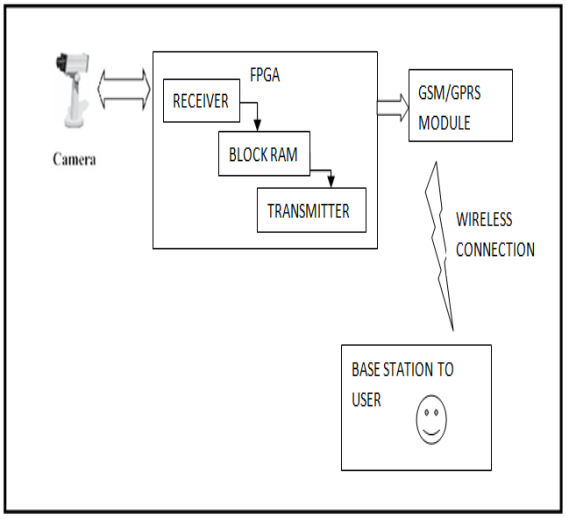

Fig.1 Block diagram of system

A. FPGA:

The main advantage of using FPGAs for the implementation of image processing applications is because their structure is able to exploit spatial and temporal parallelism. FPGA implementations have the potential to be parallel using a mixture of these two forms. For example, the FPGA could be configured to partition the image and distribute the resulting sections to multiple pipelines all of which could process data concurrently. Such parallelization is subject to the processing mode and hardware constraints of the system . VIRTEX5 FPGA is used as the processing core for the system. The Virtex™-5 family provides the newest most powerful features in the FPGA market.Virtex-5 FPGAs offer the best solution for addressing the needs of high-performance logic designers, high-performance DSP designers, and high-performance embedded systems designers with unprecedented logic, DSP,hard/soft microprocessor, and connectivity capabilities. The Virtex-5 LXT, SXT, and FXT platforms include advanced high-speed serial connectivity and link/transaction layer capability. The Viretex5 is used to design a module that will control the acquisition of image using the USB camera stores the image in memory created using block RAM and finally a transmitter created to give the data to GSM module serially and send it commands for further actions.

B. USB Webcam:

iball C8.0 webcam is used to get the images of required sector to be monitored. The webcam has a frame rate of 30 frames/sec. it provides a wide range of resolution options like 160x120, 320x240, 720x640, 1024x786,etc.It has High quality ¼" CMOS sensor, with 480k pixel sensor resolution andUSB 2.0 interface.the webcam is USB bus powered. The webcam has night light giving clear view at light. It is a plug n play type camera directly getting interfaced with processer. Here we are using resolution of 320x240 considering all aspects of memory and transmission.the data is given to processor serially.

C. Memory:

A memory block is created using block RAM of VIRTEX5 that can be used to store the acquired image before sending it for transmissionVirtex-5 devices feature a large number of 36 Kb block RAMs. Each 36 Kb block RAM contains two independently controlled 18 Kb RAMs. Block RAMs are placed in columns, and the total number of block RAM memory depends on the size of the Virtex-5 device. Total 48 blocks of 36KB block RAMs are available in VIRTEX5 giving total memory of 1728Kb. A memory of 90KB is created that could easily store the image. To make this memory 5 blocks of 18Kb are used. Everytime the image is written on the memory from first address overwriting the previous image. The size of memory can be increased if large image is to be stored upto a given limit.

D. GSM/GPRS Module:

SIM300 is used in GSM module for transmitting data from the processor to base station an form of MMS. The MMS has the image taken by the camera.

IV. IMPLEMENTATION OF SYSTEM

The webcam is given command to take the image after the specified time interval and give it to processor. Image acquisition module is implemented in the FPGA that transfers the image taken by webcam to receiver block in main processer.

The receiver block accepts the data in byte format and stores it in the memory created. The memory is of dimension 90x8 thus making it easy to store the byte data into the memory. The address is incremented automatically and beginning each frame from address zero overwriting the previous data after transmission.

The data is given to GSM/GPRS module using transmitter in the main processer module. The data is read from the memory byte by byte similarly as the data is written.

AT commands are given to the GPRS module to send the image to respective user in form of MMS. First a connection is to be checked with the module using AT commands and then image is given to send via MMS.
The complete system prototype is shown below

Fig 2. Prototype of complete system

V. RESULTS

The modules are implemented on the VIRTEX5 using Xlinx13 version and the RTL of the same till two levels are shown as below giving an idea of implementation of each block on FPGA with its each input and output.

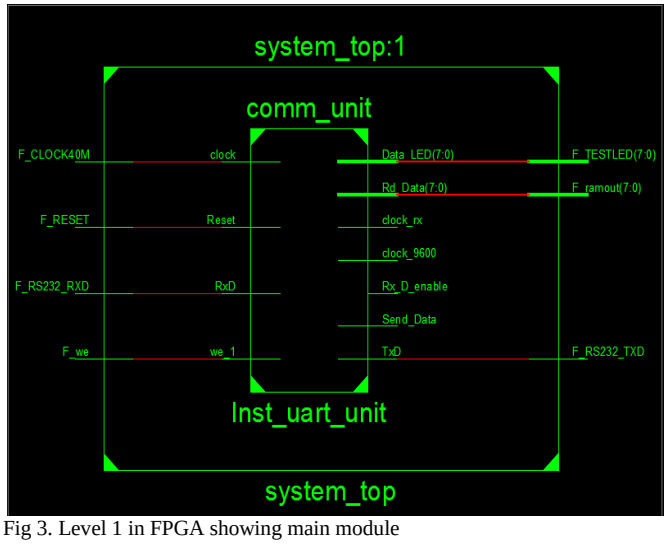

Fig 3. Level 1 in FPGA showing main module

The second level shows interconnection between each block and the various modules created to implement the system.

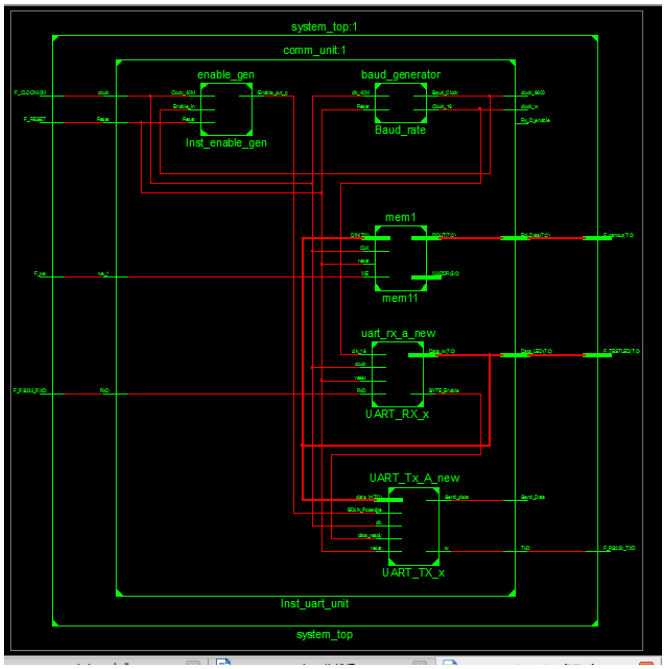

Fig 4. Level 2 showing blocks inside main module

The received image in MMS which will be the final image at the main user or person incharge.

VI. COMPLICATIONS AND FUTURE IMPLEMENTATIONS

The present node developed sends the data without compression. If better image resolution is to be taken, memory may be insufficient thus creating need for image compression on FPGA. The JPEG compression can be implemented. The node can be made smart node by implementing image comparison and sending only required image rather than every image.

VII. CONCLUSION

The paper describes the design and implementation of a wireless vision sensor. Most of the system is implemented on the Virtex5 FPGA. The image acquisition and wireless transmission module are connected to the FPGA and controlled by the same. Memory and communication link is established in the same processer instead of using different processers for each block. Large block RAM memory and programmable blocks make it possible for the implementation of single unit as compared to other processers. And reprogrammable property help for improvement and additions further.

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