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MODEL MECHANISM OF CMOS DEVICE FOR RELIBILITY ENHANCEMENT

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Abstract

This paper present specific device level life time calculation based on reliability models for the most severe failure mechanism of CMOS and analyzes the impact of different factor on lifetime distribution for the CMOS device. Also point out importance of the involvement of design and manufacturing team in achieving reliability of CMOS device.

Keywords: CMOS. TDDB. NBTI. HCI. EM.

Introduction

Voltage and temperature are two important stresses in CMOS device reliability analysis especially in accelerated testing. We focused on voltage and temperature acceleration effects towards single failure mechanism extrapolation of system voltage and temperature acceleration factor from individual failure mechanism. although various model have been proposed to describe the voltage acceleration effect for single failure mechanism . E.g. electromigration (EM), hot carrier injection(HCI), time dependent dielectric breakdown (TDDB), and negative bias temperature instability (NBTI).

An example is a high temperature CMOS foundry process which is specified for junction temperatures up to 448K as required by automotive applications. The lifetime evaluation at this stress temperature will result in a too pessimistic assessment in many cases since temperature and bias will either not occur in combination or the maximum temperature will only occur for short times. The impact of the operating conditions on the device lifetime needs to be modeled to prevent such an underestimation. The presented approach enables an application specific lifetime prediction which is based on lifetime models that are already determined within normal reliability tests. The absence of any additionally required investigations to the standard qualification procedures makes the method very attractive for foundry companies.

Model Extraction

During wafer-level qualification of the CMOS process, reliability investigations at different elevated operating conditions were performed. The reliability analysis included tests on MOS transistors as well as on further components of the process offering as capacitances and metallization. The lifetime at stress conditions was determined with respect to a defined maximum shift of a device characteristic. By using a lifetime model the lifetime finally was extrapolated to the target operating conditions. The lifetime models including the measured model parameters were taken as a base for the reliability simulation. An overview of the implemented lifetime models. The model parameters represent the worst case which has been found with respect to the variation of the CMOS process as well as to the design and to the bias conditions. For example, in terms of Hot Carrier Injection (HCI) analysis of MOS transistors, devices of minimum channel length have been stressed at maximum drain voltage and at gate voltage according to the maximum of degradation. on a device lifetime at maximum operating conditions (respectively worst case

within the specified range of operating conditions) and a lifetime model, the simulator recalculates the device lifetime (effective lifetime) according to a given set of operating conditions (mission profile).
Therefore a statical approach is used; the transition phases between the different operating points are not considered. The mission profile is broken down to different operating phases. The adjustable parameters of each phase are the maximum junction temperature T, the percentage X of the operating time with respect to the total operating time as well as the operating voltages Vds (drain-source) and Vgs (gate source) in terms of MOS transistors, the operating voltage V in terms of capacitances or the operating current density J in terms of metallization, including a duty factor for each operating condition. Dependent on the selected device category, the lifetime model is applied in order to calculate the acceleration factor *AF* which is defined as the ratio of lifetime at use conditions and lifetime at worst case conditions. For each operating phase, AF is determined by the relation of the operating conditions at use case and at worst case. The equations for the acceleration factors of the different considered degradation mechanisms are given by table 1. The effective lifetime factor of an operating phase i is then simply described by

EFi = AFi * Xi. □

A sum approach as a rough method of integration is used to calculate the total effective lifetime factor and the effective lifetime, EF = i(EFi) and tlife = t0/EF. Since the calculation of the acceleration factors is realized separately for different degradation mechanisms which all affect one device, the respective calculated effective lifetimes need to be combined. If all mechanisms affect the same device parameter (an example is the degradation of an interconnect due to Electro Migration (EM) and Stress Migration (SM) which both influence the resistance), the Sum-Of-Failure-Rate (SOFR) approach is used Otherwise, if different device parameters are affected by different mechanisms, the effective lifetimes are calculated separately. The effective lifetime factor relates to an average junction temperature Tav, which can be calculated either from Tav = i(Xi*Ti) (not thermally activated mechanism) or by solving the equation AF(Tav) = EF. In addition to pure device-level reliability estimation, the
tool also includes a failure rate calculation which is based on circuit-level tests. According to a defined average junction temperature the estimated failure rate is calculated. A simple Arrhenius model is used to consider the temperature dependence of the failure rate.

$$AF_T = \exp[\frac{E_a}{k}(\frac{1}{T_0} - \frac{1}{T_A})]$$

Where Ea is the activation energy, k is Boltzmann constant, TA is accelerated temperature, and T0 is nominal operating temperature. AFV is modeled by the exponential law:

$$AF_V = \exp[\gamma(V_A - V_0)]$$

Where is the voltage acceleration coefficient, VA is the accelerated voltage, and V0 is the nominal operating voltage. This multiplication model gains popularity because it is easy to apply reliability projections without building a lifetime model that fits a range of temperatures and voltages. However, companies usually neglect the multiple-failure-mechanisms' effect at the system level and simply assume Ea and _ are stress-independent. They only provide one Ea for AFT and one for AFV at each technology generation. Without solid proof, this kind of practice only provides rough reliability estimation, which is not enough to fully exploit the tradeoffs between performance and reliability. Simulation shows that Ea and depend on stress voltage and temperature when multiple intrinsic failure mechanisms are involve Device scaling also increases susceptibility to another

failure mechanism, NBTI, which occurs primarily in p-channel metal oxide semiconductors (PMOSFETs) with a negative gate voltage bias. The interface-trap density generated by NBTI has an inverse proportionality to oxide thickness (Tox), which means NBTI becomes more severe for ultrathin oxides while the Microelectronic System Reliability NBTI-generated fixed charge has no thickness dependence. Like NBTI for a p-channel metal oxide semiconductor (PMOS), HCI induces interface states and causes degradation of n-channel MOSFETs (NMOSFETs). Although well contained by channel engineering, it still shows up in real applications .

Failure Mechanism Lifetime Models

To model system reliability, all of the intrinsic failure mechanisms should be considered since any one of them might cause system failure. Various lifetime models have been proposed for each failure mechanism. As the goal is to show the unique characteristics of system lifetime and voltage and temperature acceleration, we will adapt the generally accepted models here. Failure rate model and acceleration factors for EM, HCI, TDDB, and NBTI are listed below.

1. EM

From the well known Black's equation and Arrhenius model, failure rate of EM can be expressed as:

$$\lambda_{EM} \propto (J)^n \cdot \exp[\frac{-E_{aEM}}{kT}]$$

Where J is the current density in the interconnect, k is Boltzmann's constant, T is absolute temperature in Kelvin, Ea is the activation energy, and n is a constant. Both Ea and n depend on the interconnect metal. Recently, copper/low-K dielectric material has been rapidly replacing aluminum alloy/SiO2-based interconnect. For copper, n has been reported to have values between 1 and 2 and Ea varies between 0.7 eV and 1.1 eV

In Equation current density, J, can be replaced with a voltage function :

$$J = \frac{C \cdot V_D}{W \cdot H} \cdot f \cdot p$$

Where C, W, and H are the capacitance, width, and thickness of the interconnect, respectively. f is the frequency and p is the toggling probability; therefore, EM is also a function of voltage:

$$\lambda_{EM} \propto (V_D)^n \cdot \exp[\frac{-E_{aEM}}{kT}]$$

The EM acceleration factor is:

$$AF_{EM}^{V_O,T_O;V_A,T_A} = (\frac{V_A}{V_O})^n \cdot \exp[\frac{E_{aEM} \cdot (T_A - T_O)}{k \cdot T_A \cdot T_O}]$$

HCI

Based on the empirical HCI voltage lifetime model proposed by Takeda and the Arrhenius relationship, HCI failure rate HCI can be modeled as:

$$\lambda_{HCI} \propto \exp[\frac{-\gamma_{HCI}}{V_D}] \cdot \exp[\frac{-E_{aHCI}}{kT}]$$

Where HCI is a technology-related constant and Ea HCI is the activation energy, which varies between 0.1 eV to 0.2 eV. The negative activation energy means HCI becomes worse at low temperature. The HCI acceleration factor is:

$$AF_{HCI}^{V_O,T_O;V_A,T_A} = \exp[\gamma_{HCI}\frac{(V_A - V_O)}{V_A \cdot V_O}] \cdot \exp[\frac{E_{aHCI} \cdot (T_A - T_O)}{k \cdot T_A \cdot T_O}]$$

TDDB

The exponential law for TDDB failure-rate voltage dependence has been widely used in gate oxide reliability characterization and extrapolation. Combining with the Arrhenius relationship for temperature dependence, the TDDB failure rate is:

$$\lambda_{TDDB} \propto \exp[\gamma_{TDDB} \cdot V_G] \cdot \exp[\frac{-E_{aTDDB}}{kT}]$$

where TDDB is a device-related constant and Ea TDDB is the activation energy. Ea TDDB normally falls in the range of 0.6 eV to 0.9 eV . The TDDB acceleration factor is:

$$AF_{TDDB}^{V_O,T_O;V_A,T_A} = \exp[\gamma_{TDDB} \cdot (V_A - V_O)] \cdot \exp[\frac{E_{aTDDB} \cdot (T_A - T_O)}{k \cdot T_A \cdot T_O}]$$

NBTI

Like TDDB, NBTI voltage dependence can also be modeled by the exponential law Considering the temperature dependence together, the NBTI failure rate is:

$$\lambda_{NBTI} \propto \exp[\gamma_{NBTI} \cdot V_G] \cdot \exp[\frac{-E_{aNBTI}}{kT}]$$

where NBTI is a constant, and Ea NBTI is the activation energy, which has been reported to vary from 0.1 eV to 0.84 eV . The NBTI acceleration factor is:

$$AF_{NBTI}^{V_O,T_O;V_A,T_A} = \exp[\gamma_{NBTI} \cdot (V_A - V_O)] \cdot \exp[\frac{E_{aNBTI} \cdot (T_A - T_O)}{k \cdot T_A \cdot T_O}]$$

Voltage and Temperature Acceleration

In a simplified example, assuming there is no interaction among failure mechanisms, the system's failure rate can be obtained by the sum-of-failure-rates since all failure mechanisms may contribute to microelectronic failures

$$\lambda_S = \lambda_{EM} + \lambda_{HCI} + \lambda_{TDDB} + \lambda_{NBTI}$$

The simulation approach is demonstrated using an inverter circuit as an example. Includes the relevant device characteristics of the NMOS and the PMOS which are part of the inverter. The devices are offered by a high-temperature CMOS foundry process and specified for junction temperatures up to 448K and operating voltages |Vdsmax| = |Vgsmax| = 5.5V. A typical automotive mission profile (motor control) contains the following operating phases:

1) *T1* = 233K, *X1* = 5%, non working mode
2) *T2* = 298K, *X2* = 20%, working mode
3) *T3* = 378K, *X3* = 65%, working mode
4) *T4* = 448K, *X4* = 10%, working mode

It is assumed that during the non working mode the bias is set to zero and during the working mode Vds and Vgs are applied with a duty cycle of 2% respectively 50%. If the peak voltages are equal to Vdsmax and Vgsmax, the effective operating lifetime calculated for the temperature mission profile is 1.0E+05h for the NMOS and the PMOS, what corresponds to an increase by a factor 50 respectively 10 compared to the worst case approximation. The calculated average junction temperatures are 362K (NMOS) and 414K (PMOS). The difference shows that the PMOS degradation is significantly more temperature accelerated than the NMOS degradation according to the implemented models. The simulated lifetime meets automotive requirements and could be further increased if reducing the peak values of Vds respectively Vgs during operation.

CONCLUSION

The presented approach enables a lifetime simulation which is based on conventional device-level reliability tests. The benefit is a more realistic assessment of device reliability during circuit operation than represented by the lifetime measured during statical stress tests. Especially the aspect of Different temperature environments can be considered accurately. Further the reliability simulation enables design optimization regarding the bias conditions (voltage, current).

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